In the Claims:

1-7. CANCELLED

8. (currently amended) A semiconductor device, comprising:

a first leadframe portion having a plurality of leads that surround a cavity, wherein the first leadframe portion has a first thickness that is about 8 mils;

a second leadframe portion attached to the first leadframe portion, the second leadframe portion having a die paddle received within the cavity of the first leadframe portion, wherein the second leadframe portion has a second thickness that is about 20 mils;

an integrated circuit die attached to the die paddle using a high temperature die attach process, located within the cavity and surrounded by the plurality of leads, the die including a plurality of die pads; and

a plurality of wires electrically connecting respective ones of the die pads with corresponding ones of the leads, wherein the wires are connected to the leads using a low temperature wire bonding process.

9. (original) The semiconductor device of claim 8, further comprising an encapsulant covering a top surface of the integrated circuit die, the wires, and the a top surface of the leads, wherein at least a bottom surface of the leads and a bottom surface of the second leadframe portion are exposed.

10. (original) The semiconductor device of claim 9, wherein the first and second leadframe portions are formed of copper.

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13. (original) The semiconductor device of 8, wherein the first and second leadframe portions are electrically isolated from each other.

14. (currently amended) A semiconductor device, comprising:

a first metal leadframe portion having a plurality of leads surrounding a cavity, wherein the first leadframe portion has a first thickness that is about 8 mils;

a second metal leadframe portion attached to the first leadframe portion and electrically isolated therefrom, the second leadframe portion having a die paddle received within the cavity, wherein the second leadframe portion has a second thickness that is about 20 mils ~~greater than the first thickness~~;

an integrated circuit die attached to the die paddle using a high temperature die attach process, located within the cavity and surrounded by the plurality of leads, the die including a plurality of die pads;

a plurality of wires electrically connecting respective ones of the die pads with corresponding ones of the leads, wherein the wires are connected to the leads using a low temperature wire bonding process; and

an encapsulant covering a top surface of the integrated circuit die, the wires, and a top surface of the leads, wherein at least a bottom surface of the leads and the second leadframe are exposed.

15. (original) The semiconductor device of claim 14, wherein the first and second leadframe portions are formed of copper.

16. (withdrawn) A method of packaging a semiconductor device comprising the steps of:

providing a first leadframe portion having a perimeter that defines a cavity and a plurality of leads extending inwardly from the perimeter, wherein the first leadframe portion has first and second sides and a first thickness;

applying an adhesive to a first side of the first leadframe portion;

providing a second leadframe portion including a die paddle having first and second surfaces and a second thickness;

attaching a semiconductor die to the second surface of the die paddle, wherein the semiconductor die has a plurality of bonding pads on a surface thereof;

stacking the second leadframe portion on the first leadframe portion such that the first surface of the die paddle is received within the cavity and contacts the adhesive;

electrically connecting the plurality of die bonding pads with respective ones of the plurality of leads with a plurality of wires;

forming a mold compound over the second side of the second leadframe portion, the semiconductor die, and the electrical connections; and

removing the adhesive from the first side of the first leadframe portion and from the first surface of the second leadframe portion so that the leads and the first surface of the second leadframe portion are exposed.

17. (withdrawn) The method of packaging a semiconductor device of claim 16, wherein the electrically connecting step comprises a wirebonding process.

18. (withdrawn) The method of packaging a semiconductor device of claim 16, wherein the second thickness is greater than the first thickness.

19. (withdrawn) The method of packaging a semiconductor device of claim 16, wherein the first thickness is about 8 mils and the second thickness is about 20 mils.

20. (withdrawn) The method of packaging a semiconductor device of claim 16, wherein the first and second leadframe portions are formed of a metal or metal alloy.

21. (withdrawn) The method of packaging a semiconductor device of claim 20, wherein first and second leadframe portions are formed of copper.

22. (withdrawn) The method of packaging a semiconductor device of claim 16, wherein the first and second leadframe portions are electrically isolated from each other.

23. (withdrawn) The method of packaging a semiconductor device of claim 16, wherein the adhesive applying step comprises applying an adhesive tape to the first side of the first leadframe portion.

24. (withdrawn) The method of packaging a semiconductor device of claim 16, wherein the die attaching step comprises attaching the die to the die paddle with a solder paste.

25. (withdrawn) The method of packaging a semiconductor device of claim 16, wherein the die attaching step comprises attaching the die to the die paddle with epoxy.

26. (withdrawn) A method of packaging a plurality of semiconductor devices, comprising the steps of:

providing a first leadframe panel, the first leadframe panel having a plurality of first leadframe portions, each having a perimeter that defines a cavity and a plurality of leads extending inwardly from the perimeter, wherein the first leadframe panel has first and second sides and a first thickness;

forming a first mating structure along an outer perimeter of the first leadframe panel;

applying an adhesive to a first side of the first leadframe panel;

providing a second leadframe panel, the second leadframe panel including a plurality of second leadframe portions, each including a die paddle having first and second surfaces and a second thickness;

forming a second mating structure along an outer perimeter of the second leadframe panel;

attaching a plurality of semiconductor die to respective ones of the second surfaces of the die paddles, wherein each of the semiconductor die has a plurality of bonding pads on a surface thereof;

stacking the second leadframe panel on the first leadframe panel such that the first surfaces of the die paddles are received within respective ones of the cavities and contact the adhesive, and the first and second mating structures mate with each other;

electrically connecting the plurality of die bonding pads of the die with respective ones of the plurality of leads of respective ones of the first leadframe portions with a plurality of wires;

forming a mold compound over the second surface of the second leadframe panel, the die and the electrical connections; and

performing a singulation operation that separates the plurality of first and second leadframe portions from the leadframe panels, thereby forming individual packaged devices.

27. (withdrawn) The method of packaging a plurality of semiconductor devices of claim 26, further comprising the step of removing the adhesive from the first side of the first leadframe panel and from the first surfaces of the second leadframe portions so that the leads and the first surfaces of the second leadframe portions are exposed.

28. (withdrawn) The method of packaging a plurality of semiconductor devices of claim 26, wherein the electrically connecting step comprises a wirebonding process.

29. (withdrawn) The method of packaging a plurality of semiconductor devices of claim 26, wherein the second thickness is greater than the first thickness.

30. (withdrawn) The method of packaging a plurality of semiconductor devices of claim 29, wherein the first thickness is about 8 mils and the second thickness is about 20 mils.

31. (withdrawn) The method of packaging a plurality of semiconductor devices of claim 26, wherein the first and second leadframe panels are formed of a metal or metal alloy.

32. (withdrawn) The method of packaging a plurality of semiconductor devices of claim 31, wherein first and second leadframe panels are formed of copper.

33. (withdrawn) The method of packaging a plurality of semiconductor devices of claim 26, wherein the first and second leadframe portions are electrically isolated from each other.

34. (withdrawn) The method of packaging a plurality of semiconductor devices of claim 33, wherein the first mating structure comprises a series of moats and the second mating structure comprises a series of dams, wherein when the first and second leadframe panels are stacked, ones of the series of dams fit within respective ones of the series of moats.

35. (withdrawn) The method of packaging a plurality of semiconductor devices of claim 34, wherein the moat and dam structure prevents mold compound bleeding during the mold compound forming step.

36. (currently amended) A semiconductor device, comprising:

a first metal leadframe portion having a plurality of leads surrounding a cavity, wherein the first leadframe portion has a first thickness that is about 8 mils;

a second metal leadframe portion attached to the first leadframe portion and electrically isolated therefrom, the second leadframe portion having a pair of adjacent die paddles received within the cavity, wherein the second leadframe portion has a second thickness that is about 20 mils ~~greater than the first thickness~~;

first and second integrated circuit die attached to respective ones of the die paddles using a high temperature die attach process, located within the cavity and surrounded by the plurality of leads, the first and second die each including a plurality of die pads;

a plurality of wires electrically connecting respective ones of the die pads of the first and second die with corresponding ones of the leads, wherein the wires are connected to the leads using a low temperature wire bonding process; and

an encapsulant covering a top surface of the first and second integrated circuit die, the wires, and a top surface of the leads, wherein at least a bottom surface of the leads and the second leadframe are exposed.